WHAT IS CLAIMED IS:

1. A method of manufacturing a semiconductor device, the method comprising:

forming a polysilicon gate electrode precursor, having first side surfaces at a first width and an first upper surface at a first height, over a mean surface of the semiconductor substrate with a gate insulating layer therebetween;

selectively oxidizing the first side surfaces and the upper surface of the polysilicon gate electrode precursor to form oxidized layers thereon; and

removing the oxidized layers from the polysilicon gate electrode precursor to form a polysilicon gate electrode having second side surfaces at a second width less than the first width and a second upper surface at a second height less than the first height.

2. The method according to claim 1, comprising forming nitride layers on the main surface of the semiconductor substrate on each side of the polysilicon gate electrode precursor.

3. The method according to claim 2, comprising:

forming an oxide layer on the main surface of the semiconductor substrate;

forming a layer of polysilicon on the oxide layers;

patterning to form the polysilicon gate electrode precursor with a gate oxide layer thereunder and extending on the main surface of the semiconductor substrate; and

forming the nitride layers on the gate oxide layer extending on the main surface of the semiconductor substrate.

4. The method according to claim 2, comprising:

ion implanting impurities, using the polysilicon gate electrode precursor as a mask, to form deep source/drain regions;

forming the nitride layers on the main surface of the semiconductor substrate over the deep source/drain regions;

selectively oxidizing the side surfaces and upper surface of the polysilicon gate electrode precursor to form the oxidized layers thereon;

removing the oxidized layers from the silicon gate electrode precursor to form the polysilicon gate electrode;

removing the nitride layers; and

ion implanting impurities, using the polysilicon gate electrode as a mask, to form source/drain extensions.

5. The method according to claim 4, further comprising:

forming dielectric sidewall spacers on side surfaces of the polysilicon gate electrode; and

forming metal silicide layers on the upper surface of the polysilicon gate electrode and on the main surface of the semiconductor substrate over the deep source/drain regions.

6. The method according to claim 5, comprising forming silicon nitride sidewall spacers as the sidewall spacers on the side surfaces of the polysilicon gate electrode.

7. The method according to claim 6, comprising:

forming an oxide liner on the second side surfaces of the polysilicon gate electrode and on a portion of the main surface of the semiconductor substrate; and

forming the silicon nitride sidewall spacers on the oxide liner.

8. The method according to claim 1, comprising forming the polysilicon gate electrode at a second height less than 1,000 Å and at a second width less than 500 Å.

9. The method according to claim 8, comprising forming the polysilicon gate electrode precursor at a first height greater than 1,000 Å and at a first width greater 500 Å.

10. The method according to claim 9, comprising forming the polysilicon gate electrode at a second height of 300 Å to 900 Å and at a second width of 150 Å to 400 Å.

11. The method according to claim 4, comprising forming the polysilicon gate electrode at a second height less than 1,000 Å and at a second width less than 500 Å.

12. The method according to claim 11, comprising forming the polysilicon gate electrode precursor at a first height greater than 1,000 Å and at a first width greater than 500 Å.

13. The method according to claim 12, comprising forming the polysilicon gate electrode at a second height of 300 Å to 900 Å and at a second width of 150 Å to 400 Å.

14. The method according to claim 11, further comprising:

forming silicon nitride sidewall spacers on the second side surfaces of the polysilicon gate electrode; and

forming metal silicide layers on the second upper surface of the polysilicon gate electrode and on the main surface of the semiconductor substrate over the deep source/drain regions.

15. The method according to claim 14, comprising:

forming an oxide liner on the second side surfaces of the polysilicon gate electrode and on a portion of the main surface of the semiconductor substrate; and

forming the silicon nitride sidewall spacers on the oxide liner.